Notice of Allowability	Application No.	Applicant(s)	
	10/717,934	TERUI ET AL.	
	Examiner	Art Unit	
	William M. Brewster	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3 January 2006*.

2. ☒ The allowed claim(s) is/are *1,2,6-12 and 19-30*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *022806* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andrew J. Telesz, JR. (Reg. No. 33,581) on 2 February 2006.

The application has been amended as follows:

a) In the Title

After "Layer" insert --Including Forming Scribe Lines and Dicing--

b) In the Claims

Cancel claims 3-5, 31, and 32.

Claim 1 (Currently Amended): A method of fabricating a semiconductor device comprising:

providing a semiconductor wafer having a substrate with a first surface and a second surface opposite of the first surface, the first surface having a plurality of circuit elements each of which is defined by scribe lines formed in the substrate;

forming a sealing resin on the first surface of the substrate;

forming a plurality of external terminals on the first surface of the substrate, wherein the external terminals respectively electrically connect to the circuit elements and project from the sealing resin;

forming a metal heat conduction film on the second surface of the substrate;

forming a heat spreading material on the metal heat conduction film ~~second surface of the substrate, after said forming the sealing resin~~; and

separating the semiconductor wafer by cutting the substrate at the scribe lines after the heat spreading material is formed on the metal heat conduction film ~~second surface of the substrate~~.

Claim 2 (Currently Amended): The method according to the claim 1, further comprising polishing the second surface of the substrate before said forming a metal heat conduction film ~~the heat spreading material~~.

In claim 21, line 2, delete "on" and insert --over--

In claim 22, line 2, delete "on" and insert --over--

In claim 23, line 3, delete "on" and insert --over--

Claim 29 (Currently Amended): A method of fabricating a semiconductor device comprising:

providing a semiconductor wafer having a substrate with a first surface and a second surface opposite of the first surface, the first surface having a plurality of circuit elements each of which is defined by scribe lines formed in the substrate;

forming a sealing resin on the first surface of the substrate;

forming a plurality of external terminals on the first surface of the substrate, wherein the external terminals respectively electrically connect to the circuit elements and project from the sealing resin;

forming a metal heat conduction film on the second surface of the substrate;

forming a material film that covers the metal heat conduction film ~~second surface of the substrate~~, the material film having a heat radiating ratio that is greater than a heat radiating ratio of the substrate; and

separating the semiconductor wafer by cutting the substrate at the scribe lines after [[the]] said forming a material film ~~is formed on the second surface of the substrate~~.

Rejoinder of Claims

Claims 1, 2, 6, 19-30 are directed to an allowable product. Pursuant to the procedures set forth in the Official Gazette notice dated March 26, 1996 (1184 O.G. 86), claims 7-12, directed to the process of making or using the patentable product, previously withdrawn from consideration as a result of a restriction requirement, are now subject to being rejoined. Claims 7-12 are hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Since all claims previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, the restriction requirement made in the Office action mailed on 29 December 2004 is hereby withdrawn.

Reasons for Allowances

The following is an examiner's statement of reasons for allowance: whereas Akram, US Patent No. 6,544,821 B2 teaches in fig. 4, forming a wafer with plurality of circuit elements, scribe lines formed in the substrate 25, in fig. 6, sealing resin 30, external terminals project from the sealing resin 18, material layer formed on the second

surface 34, and in fig. 7, separating the semiconductor wafer, Akram does not teach the features as amended in claims 1 and 29 above. Akram also does not teach the features enumerated in claim 6, 11-13, "selectively forming a heat spreading material on the second surface of the semiconductor wafer, after said forming the sealing resin, wherein the scribe lines are exposed from the heat spreading material." The prior art of record fails to teach, in combination, the process features.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William M. Brewster whose telephone number is 571-272-1854. The examiner can normally be reached on Full Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Brewster

WILLIAM M. BREWSTER
PRIMARY EXAMINER

28 February 2006
WB